The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

SpaceWire-RT project latest news	Newsletter #2: 20.05.2013

Dear Sir or Madam,

This is the second newsletter of the SpaceWire-RT FP7 project.

It has been sent to you because you or your company is interested in the results of our project and asked to be on the SpaceWire-RT mailing list.

Web-site information:

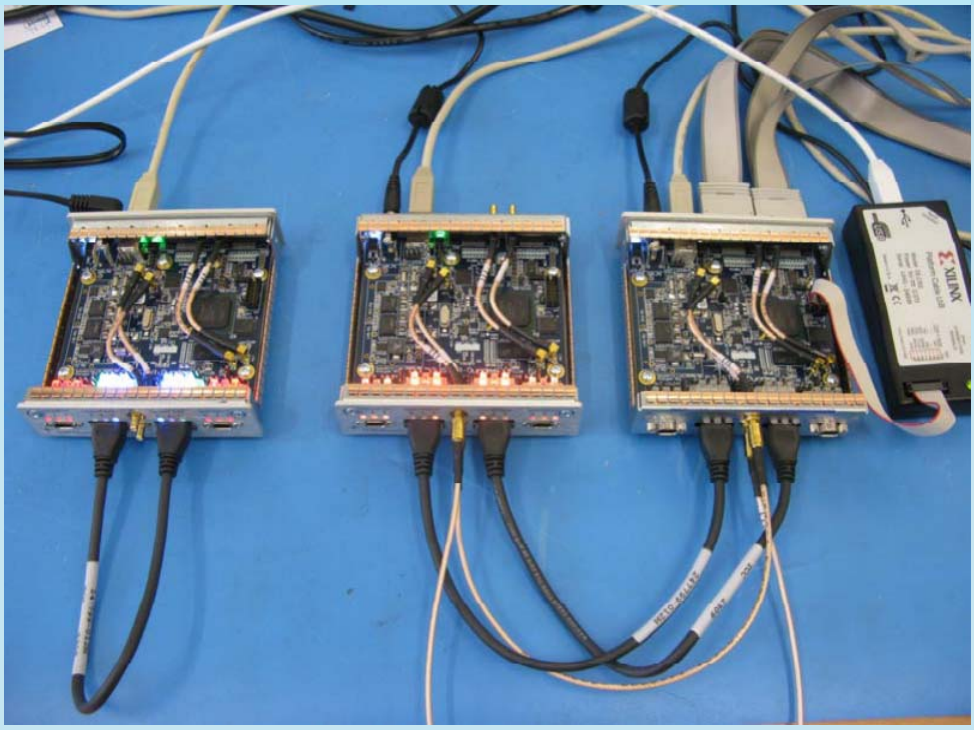
LATEST SPACEWIRE-RT NEWS

What is SpaceWire-RT?

The trend towards "Operationally Responsive Space", where spacecraft can be rapidly assembled, configured and deployed, to meet specific mission needs, e.g. disaster support, requires flexible on board communication networks with plug-and-play capability. The growing autonomy of scientific missions to remote planets requires networks that are robust and durable, able to recover from transitory errors and faults automatically. The importance of spacecraft mass reduction motivates the sharing of networks for payload data-handling and avionics. Avionics and robotics impose requirements on network responsiveness and determinism. Increasing international collaboration on scientific and Earth observation spacecraft requires standard network technology where a component developed by one nation will interoperate effectively with equipment developed by another. **SpaceWire-RT**, a project funded under the EU's Seventh Framework Program (FP7), aims to fulfill these demanding requirements with a flexible, robust, responsive, deterministic and durable standard network technology that is able to support both avionics and payload data-handling applications. The creation of SpaceWire-RT technology will substantially strengthen collaborative bonds between the Russian and European organisations involved in the research, and lead to technology of vital importance for future space missions.

The principle aims of SpaceWire-RT are:

- Support all or most spacecraft onboard communication requirements:
  - – Instrument interfacing
  - – Device and sub-system networking
  - – Inter-processor communications
  - – Gathering housekeeping information
  - – Deterministic command and control
  - – Time distribution
  - – Sub-system synchronisation
  - – Event signalling
- Provide a coherent set of protocols covering:
  - – Full range of operational speeds (1 Mbit/s to 20 Gbit/s)
  - – Full range of operational distances (0.1 m to 100 m)
  - – Using a range of physical media and signals



Prototype SpaceWire-RT Equipment

SPACEWIRE-RT CURRENT PROGRESS

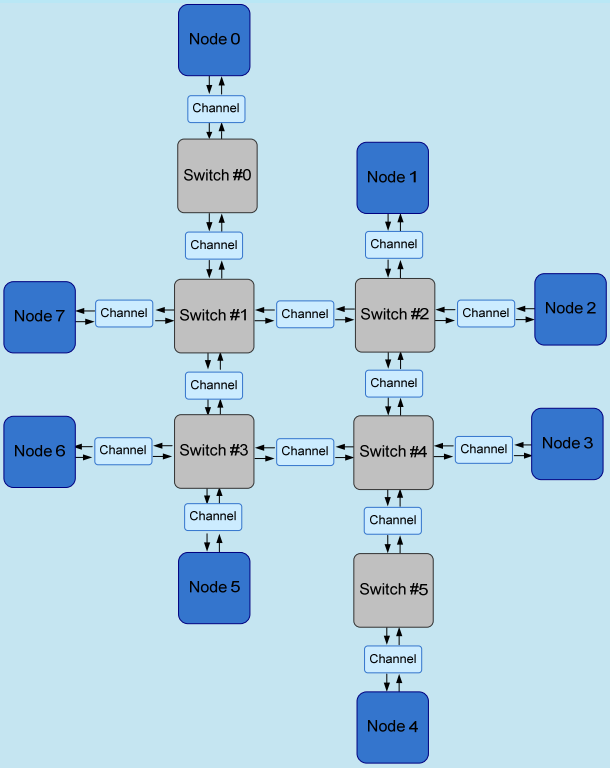
Since the last newsletter, activities have been focused on Validation and Simulation of the SpaceWire-RT Outline Specification (Work Package 3), design and validation of a VHDL IP Core for SpaceWire-RT (Work Package 4) and evaluating the implementation of SpaceWire-RT as an ASIC Core (Work Package 5).

Work Package 3 results

Work Package 3 was successfully completed on schedule by Saint-Petersburg State University of Aerospace and Instrumentation (SUAI) in January 2013.

One of the main objectives of Work Package 3 was to check the correctness and consistency of the SpaceWire-RT specification. This was done by specification and simulation of the SDL point-to-point model and by simulation of the SystemC network models.

- The SDL model was primarily focused on checking the internal functionality and how all mechanisms of all layers work in common in one node.
- The SystemC network models were primarily focused on simulation and checking of network aspects of the SpaceWire-RT specification, performance parameters (e.g. latency) and some features that cannot be covered by SDL point-to-point simulation (e.g. broadcast distribution, quality of service, etc.).



Mixed configuration for SystemC network model simulation

During specification and simulation a number of documents with proposals, change requests and issues for discussion was produced by SUAI and provided to the University of Dundee (UNIVDUN). In total, SUAI produced 139 change requests. The results of Work Package 3 have made a contribution to the SpaceWire-RT Outline Specification v.2.0.

In the scope of testing SpaceWire-RT against the requirements of industry, a number of tests were performed which evaluate and check SpaceWire-RT functionality in point-to-point connection (primarily SDL model) and in networks with different topologies (SystemC model). To test basic mechanisms of the SpaceWire-RT, two different network configurations were used: point-to-point configuration and mixed configuration (tree and circular configurations combined in one network). In general, this testing has shown that SpaceWire-RT satisfies the requirements provided by industry.

Work Package 4 results

UNIVDUN have developed the architectural design of the SpaceWire-RT IP Core based on the SpaceWire-RT Outline Specification from WP2 and produced a validation plan for the SpaceWire-RT VHDL IP Core for FPGAs. This plan is based on SpaceWire-RT Requirements and Use Cases and taking into account the SDL simulation validation plan produced by SUAI in WP3. Then UNIVDUN designed the VHDL code for the Prototype SpaceWire-RT VHDL IP Core and an architecture independent Test Bench to run it on the Prototype SpaceWire-RT VHDL IP Core using the results to debug the IP Core. The result of this work was the Prototype SpaceWire-RT IP Core on an FPGA.

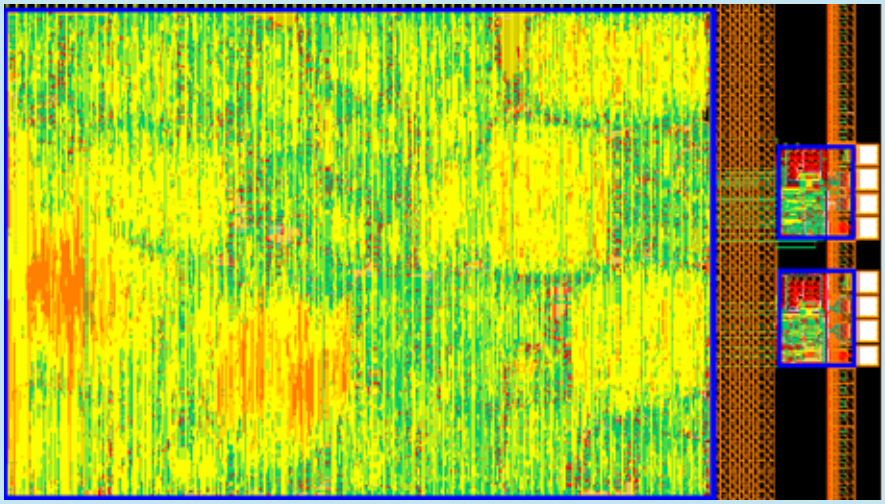
So VHDL IP Core Development has resulted in the successful implementation and testing of the QoS and FDIR capabilities of SpaceFibre. In addition an oversampling implementation using LVDS has been implemented and simulated showing the feasibility of this approach.

Work Package 5 results

ELVEES have reviewed available space qualifiable (Radiation Tolerant) ASIC Russian and European Microelectronics technologies for the area and timing parameters estimations for the ASIC technologies from 250 nm up to 65 nm.

Then the virtual design of the SpaceWire-RT ASIC IP-Core was developed based on the SpaceFibre digital controller closed Soft IP-core (implemented by UNIVDUN) and ELVEES IP-core Library from the ASIC platform MULTICORE including Soft and Hard IP-cores (8B/1B CODEC, SERDES, PLLs, transceivers). After this ELVEES produced the validation plan for the SpaceWire-RT ASIC IP-Core Verilog description taking into the account the simulation and validation plan produced by SUAI in WP3.

RTL Verilog code and a Test Bench was created for SpaceWire-RT ASIC IP-Core and it was debugged and validated using the Test Bench produced by UNIVDUN in WP 4 and the ASIC IP core Test Bench produced by ELVEES in WP5. Then the Netlist and layout of SpaceWire-RT ASIC IP - Core was synthesized on the space qualifiable ASIC technologies base.



The example of the preliminary Layout of the SpaceWire-RT ASIC IP-Core based on UNIVDUN SpaceFiber closed soft IP-core

The analysis of Working Package 5 results shows that the SpaceWire-RT RT ASIC IP-Core effectively realizable on the basis of existing Russian and European Microelectronics RT Technologies.

Feasibility analysis demonstrated:

1. The area (6.87- 8.73 mm2) of the SpaceWire-RT ASIC IP-core on the base 180nm Radiation Tolerant Libraries approximately in 3-4 times larger than SpaceWire ASIC IP-core (1-8 virtual channels), but IP-core applies all advantages in QoS, FDIR and others SpW-RT benefits. The area for the virtual channels (VCh) is about 1.78 mm2 for this 180 nm technology and will be reduced with the new Memory compiler for ELVEES RT Library.

SpaceWire and SpaceWire-RT ASIC IP- Core area estimation on the base ELVEES 180nm Radiation Tolerant Libraries

Interface	Layout Area of the digital controller, mm^2	Area of the digital-analog transceivers (Ser/Des, RX, TX), mm^2	The total area of the analog & digital IP – block, mm^2
SpaceWire	2,07	0,024 (LVDS)	2,09
SpaceWire-RT (upper estimations)			
8Ch	8,06	0,37	8,43
4Ch	7,17		7,54
2Ch	6,72		7,09
1Ch	6,50		6,87

2. The data rate of the SpaceWire-RT ASIC IP-core on the base 180 nm Radiation Tolerant Libraries today applied and proved for the PHY level on the real silicon for the one lane as 1.25 Gbps. It can be rise up to 5Gbps with 4 lanes.
3. The data rate of 10Gbps can be reached with a 4 lane SpFi-CML interface on a 130nm CMOS-process. The area estimation is 6.5 mm2 (maximum) with 8 VCh.
4. The MK180RTSC library based on the Mikron HCMOS8D technology is ready for the fabrication of the SpaceWire-RT ASIC IP-core and can be estimated as suitable for its implementing.
5. The problem of radiation-tolerant design of hard IP-transceiver unit that comply with the protocol SpW-RT/SpFi-CML (physical medium – copper line) was solved.
6. In the order to estimate the practical limits of communication range and available data rates, different samples of common cables have been S-parameters measured and their linear models developed. Analysis of eye diagram simulation results showed the possibility of data transfer rates up to 1.25 Gbps over a distance of 20 m twisted pair Category 5 for under the 180nm CMOS ASIC realization.
7. VML-driver in the developed transmitter has an adjustable power supply (1.8-3.,3 V), provides the

ability to scale without reducing output signal levels, the gain in power consumption of at least 25% in most of the operating range of rates and, if necessary, full compatibility with CML-level logic.

8. The main parameters of the transceivers IP-cores, using 180 nm CMOS technology of JSC Micron (Russia), are:

- A wide range of data rates 5 Mbps ... 1.25 Gbps (discrete series);
- Distance – up to 10 m over twisted pair Category 5;
- Power consumption no more than 150-200 mW at increasing rates in work range;
- dimensions of IP blocks of the transmitter and receiver are the same –
- 470×395 μm², square - 0.186 mm2.
- Whole Transceiver parameters are satisfied to SpFi-CML protocol.

9. The directions of further development of SpW-RT standard at the physical layer are offered. Depending on the environment and the transmission distance, rate and the feasibility (and usefulness) of the transformer isolation proposed division of all transmission systems to 5 profiles covering existing cable channels and channels within the printed circuit boards, as well as advanced fiber-optic channels.

The Physical layer profiles for SpaceWire-RT specifications proposal

Parameter	Units	Profile A	Profile B	Profile C	Profile D	Profile E
Physical medium	-	UTP cat.5	BSTP or Coax TBD	PCB	RG-58	Fiber optic
Type of decoupling	-	Transformer	Transformer	Capacitor	Capacitor	Fiber optic
Type of code	-	8B/10B	8B/10B	8B/10B	TBD	TBD
Minimum rate (necessarily)	Mbod	25	625	100	1000	TBD
Maximum rate (optional)	Mbod	125	3125	10000	10000	10000
Isolation voltage	V	1000	1000	12	50	10000+
Rate at given distance	Mbod@m	125@60 25@140	3125@15 625@35	n/a	6000@30	n/a

New version of the SpaceWire-RT Outline Specification

A new version of the SpaceWire-RT Outline Specification was produced on the basis of the results of the extensive simulation and investigation work carried out by SUAI in Work Package 3. In addition to changes referring to the simulation impact, the new version of the SpaceWire-RT Outline Specification includes the addition of new Packet and Management Layers to the stack and some results of the SpaceWire-RT Network Layer development.

In addition, the Outline Specification gives a general concept of SpaceWire to SpaceFibre Bridge which provides the opportunity to connect a legacy SpaceWire device to a SpaceFibre network.

The SpaceWire-RT Outline Specification can be downloaded by following this link: Download

SPACEWIRE-RT FINAL REVIEW MEETING

The final review meeting will be held in the European Commission in **Brussels** on the **25th of July 2013**. This meeting will be attended by the representatives of each of the SpaceWire-RT consortium members. This meeting is the final point of the SpaceWire-RT project when all the members will give presentations on the final results of the project.

CONGRATULATIONS!

Steve Parkes and Yuriy Sheynin have been awarded by the European Space Agency for Teamwork Excellence in recognition of their contribution to the development and use of the SpaceWire standard and Technology.

PRESENTATIONS AND PUBLICATIONS

The SpaceWire-RT consortium members have presented the project at a number of forums since the last newsletter:

- October 2012: “Status on the FP7/SPWRT activity” was presented at the Nineteenth SpaceWire Working Group meeting by *Steve Parkes (UNIVDUN).*
- October 2012: "Unification of onboard computational facilities architecture based on SpaceWire" for the "2nd All-Russian scientific and technical conference: Pilotless spacecraft and atmospheric vehicles control systems", Moscow Research and Design Bureau "Mars", Moscow, Russia by *Petr Eremeev, Viacheslav Grishin (SMIC).*
- November 2012: The paper on the status of the SpaceWire-RT project was published in the "Let's embrace space. Volume 2" book by *Steve Parkes (UNIVDUN).*
- November 2012: The status of the SpaceWire-RT project was presented at the "2nd FP7 Space Conference" in Larnaca by *Valentin Olenev (SUAI).*
- November 2012: "SpaceWire application for development of ROSCOSMOS" for the "XVI International Scientific Conference “RESHETNEV READINGS” dedicated to the memory of Mikhail Reshetnev, the General Designer of Aerospace Systems", Siberian State Aerospace University, Krasnoyarsk, Russia by *Viacheslav Grishin (SMIC)*.
- April 2013: “SpaceWire-RT/SpaceFibre simulation models: implementation and application” was presented at the Twentieth SpaceWire Working Group meeting by *Valentin Olenev (SUAI).*
- April 2013: “Status on the FP7/SPWRT activity” was presented at the Twentieth SpaceWire Working Group meeting by *Steve Parkes (UNIVDUN).*
- April 2013: “SpaceWire-RT IP Core ASIC feasibility analysis” was presented at the Twentieth SpaceWire Working Group meeting by *Tatiana Solokhina (ELVEES).*
- April 2013: “SpaceWire-RT copper line transceivers as a Radiation Tolerant ASIC IP-core project” was presented at the Twentieth SpaceWire Working Group meeting by *Sergey Kondratenko (ELVEES).*
- April 2013: “SpaceWire-RT standard simulation models” (in Russian) at the SUAI Scientific Session 2013 by *Valentin Olenev, Irina Lavrovskaya, Ilya Korobkov (SUAI).*
- April 2013: “Broadcast messages transmission simulation in the SpaceWire-RT network” (in Russian) at the 66th International Scientific Conference for the Students at SUAI by *Ilya Korobkov, Nicolay Sinyov, Valentin Olenev (SUAI).*
- April 2013: “SpaceWire-RT standard simulation models” at the 13th FRUCT Conference by *Valentin Olenev, Irina Lavrovskaya, Ilya Korobkov (SUAI).*
- April 2013: “Unification of spacecraft’s onboard control system based on SpaceWire and SpaceFibre” for the "International conference, “VNIIEM Corporation” JSC, Moscow, Russia" by *Sergey Gorbunov (SMIC)*.
- April 2013: “Principles of architecture of onboard control system and formation of spacecraft’s purpose-orient” for the "International conference, “VNIIEM Corporation” JSC, Moscow, Russia" by *Viacheslav Grishin (SMIC)*.

Future presentations and publications

There are a number of presentations and publications on the SpaceWire-RT standard planned in the coming months:

- May 2013: "SpaceFibre: a multi-gigabit/s network technology for spacecraft on-board data-handling applications", DASIA 2013 by *Steve Parkes (UNIVDUN).*
- June 2013: “SpaceWire-RT/SpaceFibre specification and modeling” at the 2013 SpaceWire Conference by *Valentin Olenev, Irina Lavrovskaya, Ilya Korobkov (SUAI).*
- June 2013: “SpaceFibre Quality of Service Features Support in the Network Level" at the 2013 SpaceWire Conference by *Nadezhda Matveeva, Elena Suvorova, Valentin Olenev, Irina Lavrovskaya, Ilya Korobkov, Artur Eganyan (SUAI)*.
- June 2013: “SDL and SystemC models of SpaceWire-RT protocol” (in Russian) for the

"Radioelectronics, Engineering, Technology. – 2013" by *Valentin Olenev, Irina Lavrovskaya, Ilya Korobkov (SUAI).*

- June 2013: “The second generation of the MULTIBOARD chipset based on the SpaceWire family standards development” for the "Radioelectronics, Engineering, Technology. – 2013" by *Jaroslav Petrichkovich, Tatiana Solokhina, Yury Sheynin, Sergey Kondratenko (ELVEES)*.
- June 2013: “The high-performance Multicore microprocessor with SpaceFibre based gigabit links for space applications” for the "Radioelectronics, Engineering, Technology. – 2013" by *Tatiana Solokhina, Jaroslav Petrichkovich, Alexander Glushkov, Yury Alexandrov (ELVEES)*.

Contact us

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